

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1 (original). A circuit device (1), with at least one connection (3b), to which a clock pulse (/CLK, /CLK<sub>T</sub>) can be applied, characterized in that the circuit device (1) also comprises a clock pulse detection facility (2) to determine whether there is a clock pulse (/CLK, /CLK<sub>T</sub>) present at the connection (3b).

2 (original). A circuit device (1) with at least one further connection (3a), to which a further clock pulse (CLK, CLK<sub>T</sub>) can be applied, whereby in determining whether a clock pulse (/CLK, /CLK<sub>T</sub>) is present at the connection (3b), it is determined whether there are differential clock pulses (CLK, CLK<sub>T</sub>; /CLK, /CLK<sub>T</sub>) present at the connections (3a, 3b), or whether there is a single clock pulse (CLK, CLK<sub>T</sub>) present at the further connection (3a), but not at the connection (3b).

3 (currently amended). A circuit device (1) according to Claim 1 or 2, which comprises a comparison device (24) for comparing the signal present at the connection (3b), in particular the clock pulse (/CLK, /CLK<sub>T</sub>) applied thereto, with a reference signal (VREF).

4 (original). A circuit device (1) according to claim 3, in which the comparison device (24) comprises a differential amplifier.

5 (currently amended). A circuit device (1) according to Claim 3 or 4, in which the comparison device (24) emits a pulse, more specifically a clock pulse detection signal, when the level of the signal present at the connection (3b) exceeds or falls below a predetermined level (VREF), in particular, the level of the reference signal (VREF).

6 (currently amended). A circuit device (1) according to one of ~~Claims 3 to 5~~  
Claim 3, in which the comparison device (24) emits a signal, more specifically a clock pulse detection signal, when the level of the signal present at the connection (3b) first exceeds a predetermined, first level ( $V_{REF} + \Delta U_1$ ), and then falls below a predetermined second level ( $V_{REF} - \Delta U_2$ ) that differs from the first level.

7 (currently amended). A circuit device (1) according to one of ~~Claims 3 to 5~~  
Claim 3, in which the comparison device (24) then emits a pulse, more specifically a clock pulse detection signal, when the level of the signal present at the connection (3b) first falls below a predetermined first level and then exceeds a predetermined second level that differs from the first level.

8 (currently amended). A circuit device (1) according to ~~one of the above~~  
~~claims~~ Claim 2, which also comprises a counter device (7), in particular for detecting the number of pulse, particularly clock pulse detection signals, emitted by the comparison device (24).

9 (original). A circuit device (1) according to Claim 8, in which, when the number ( $Z$ ) of pulse, in particular clock pulse detection signals emitted by the comparison device (24), and detected by the counter device (7), is larger then or equal to a predetermined number ( $Z_0$ ), it is determined that a clock pulse ( $/CLK$ ,  $/CLK_T$ ) is present at the connection (3b).

10 (currently amended). A semi-conductor component that comprises at least one circuit device (1) according to ~~one of the claims 1 to 9~~ Claim 2.

11 (original). A semi-conductor component according to Claim 10, which is a DDR (double data rate) component, in particular a DDR memory component.

12 (original). A semi-conductor component according to Claim 10, in which the memory component is a DRAM (dynamic random access memory).